CLAIMS

We claim:

1   1.   A method for verifying core determinacy, the method comprising:

2   extracting data stored in core model structures;

3   comparing the extracted data of one modeled processor core with extracted data of

4 another modeled processor core;

5   determining if any mismatching data will cause core divergence; and

6   facilitating notice of an error if any mismatching data will cause core divergence.

1   2.   The method of claim 1, wherein extracting data comprises extracting data

2 from core data storage and interconnect elements.

1   3.   The method of claim 2, wherein extracting data comprises extracting data

2 from at least one of core buffers, core caches, core queues, core state variables, core state

3 machines, and bus values.

1   4.   The method of claim 1, wherein determining comprises accessing a data

2 structure that matches divergence results with given mismatched data.

1   5.   The method of claim 1, wherein determining comprises implementing an

2 algorithm that uses the mismatched data as inputs.

1   6.   The method of claim 1, wherein facilitating notice comprises pending a check

2 for a lockstep block checker to signal when divergence occurs.

1   7.   The method of claim 6, wherein facilitating notice comprises flagging an error

2   if the lockstep block checker does not signal that divergence occurred.

1   8.   The method of claim 1, further comprising determining if a modeled processor

2   is operating in lockstep mode.

1   9.   The method of claim 8, wherein determining if a modeled processor is

2   operating in lockstep mode comprises analyzing at least one of a lockstep block and a

3   lockstep block checker.

1   10.   A system for verifying core determinacy, the system comprising:

2   means for determining if a modeled processor is operating in a lockstep mode;

3   means for extracting data stored in core model structures;

4   means for comparing the extracted data to determine if any data associated with one

5   processor core does not match data associated with another processor core; and

6   means for determining if any mismatching data will cause core divergence.

1   11.   The system of claim 10, wherein the means for determining if a modeled

2   processor is operating in a lockstep mode comprise means for analyzing at least one of a

3   lockstep block and a lockstep block checker.

1   12.   The system of claim 10, wherein the means for extracting data comprise

2   means for extracting data from core data storage and interconnect elements.

1   13.   The system of claim 10, wherein the means for determining if any

2   mismatching data will cause core divergence comprise at least one of a data structure and an

3   algorithm.

1   14.   The system of claim 10, further comprising means for pending a check for a

2   lockstep block checker to signal when divergence occurs.

1   15.   The system of claim 10, further comprising means for flagging an error.

1   16.   A determinacy checker stored on a computer-readable medium, the system

2   comprising:

3   logic configured to determine if a modeled processor is operating in a lockstep mode;

4   logic configured to extract data stored in core model structures;

5   logic configured to compare the extracted data;

6   logic configured to determine if any data associated with one processor core does not

7   match data associated with another processor core;

8   logic configured to determine if any mismatching data will cause core divergence; and

9   logic configured to facilitate notification of an error if any mismatching data will

10   cause core divergence.

1   17.   The checker of claim 16, wherein the logic configured to determine if a

2   modeled processor is operating in a lockstep mode comprises logic configured to analyze at

3   least one of a lockstep block and a lockstep block checker.

1   18.   The checker of claim 16, wherein the logic configured to extract data

2   comprises logic configured to extract data from core data storage and interconnect elements.

1   19.   The checker of claim 16, wherein the logic configured to determine if any

2   mismatching data will cause core divergence comprises logic configured to access at least

3   one of a data structure that matches divergence results with given mismatched data and an

4   algorithm that uses the mismatched data as inputs.

1   20.   The checker of claim 16, wherein the logic configured to facilitate notification

2   comprises logic configured to pend a check for a lockstep block checker to signal when

3   divergence occurs.

1   21.   The checker of claim 16, wherein the logic configured to facilitate notification

2   comprises logic configured to flag an error.

1   22.   A computer system, comprising:

2   a processing device; and

3   memory including a determinacy checker that is configured to extract data stored in

4   core model structures, compare the extracted data, determine if any mismatching data will

5   cause core divergence, and facilitate notification of an error if the mismatching data will

6   cause core divergence.

1   23.   The system of claim 22, wherein the checker is configured to extract data from

2   core data storage and interconnect elements.

1   24.   The system of claim 22, wherein the checker is configured to pend a check for

2   a lockstep block checker to signal when divergence occurs.

1   25.   The system of claim 22, wherein the checker is configured to flag an error.